DETAILED ACTION

Double Patenting

1. The Terminal Disclaimer is acknowledged. Therefore, the previous double patenting is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, and 92-95, 97-103, 105-109, 111-113, and 118 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh et al. (US 5,689,128, previously cited, hereinafter, Hshieh) and in view of Burr et al. (US 5,719,422, newly cited, hereinafter, Burr.)

In regard to claims 46, 67, and 97, in fig. 3 (one of the embodiments), Hshieh discloses a field effect transistor comprising:

a semiconductor substrate 10 or 12 having dopant of a first conductivity type, n-type;

a trench 24 extending a predetermined depth into the semiconductor substrate;

a doped well 14 having dopant of a second conductivity type, p-type, opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction at a first depth;

a doped source region 20 having dopant of the first conductivity type and extending into the semiconductor substrate to form a source junction at a second depth; and

a doped heavy body region 18 having dopant of the second conductivity type, p+, and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the depth of the trench,

wherein the heavy body forms a junction in the doped well. The gate-forming trenches 22 arranged substantially parallel to each other.

Hshieh, however, does not expressly describe the junction as an abrupt junction. It should be noted that even though the cited reference does not mention the function of the heavily doped region as abrupt junction. But the structure of the deeper doped well and a second well of an opposite dopant may create an abrupt junction as claimed since the concentration of these regions is typically different as described in the current application. In the current specification, the Applicants further admit that this abrupt junction can be formed by different methods, for example, diffusion, implantation, etc. Hshieh also teaches that the dopants are introduced in the substrate by a method of implanting the dopant. In order to justify the analisis as mentioned, Burr is incorporated herein to further explain how a such junction can be formed. For example, Burr, in fig. 1, discloses an analogous device, a low threshold voltage high performance junction

transistor transistor, and the structure includes regions of the same dopant, P-type, 46 and 34. These regions are formed by dopant implantation method and also have a typical concentrations different from each other; therefore, they form a abrupt junction therebetween in order to form a high performance device because this junction provides a low threshold voltage, and provides the growth of the depletion regions is immediately slowed. See also, Burr's col. 7, lines 25-30, and 55-55.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize the structure that could create such junction as taught by Burr in Hshieh's device in order to take the advantage as mentioned.

In regard to claims 48, 68, and 99, Hshieh further discloses that the doped well has a flat bottom. See fig. 3, for example.

In regard to claims 49, 71, and 100, wherein the trench has rounded top corners. See also, fig. 3.

In regard to claims 50, 72, and 101, wherein the trench has rounded bottoms corners. See also, fig. 3.

In regard to claims 51, 73, and 102, wherein the trench has rounded top and bottom corners. See also, fig.3.

In regard to claims 52 and 103, wherein the heavy body comprises a heavily doped region 18 formed by implanting dopants of the second conductivity type at an approximate location of the abrupt junction. See also, fig.3.

In regard to claims 54, 89, and 105, wherein the substrate comprises a first highly doped region 10 and a second doped region 34 disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region. See fig.3, where the plus sign indicates heavier concentration.

In regard to claims 55 and 106, Hshieh further discloses a terminator structure surrounding the device. See the discussion in col.3, lines 45-49.

In regard to claims 56 and 107, wherein the termination portion comprises a doped region, and it inherently creates a p/n junction therein. See also, col. 3, lines 45-49.

In regard to claims 57-58, and 108-109, in accordance with the above claim objections, wherein the termination portion conventionally contains trench. See also, col.3, lines 46-48.

In regard to claims 60-61, and 111-112, Hshieh further discloses the second doped region, region 34, has a thickness of 1-2 microns. See col. 4, lines 49-51.

In regard to claims 62-63, 92-93, and 113-114, wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately 1 micron. See col. 4, line 1 and col.4, lines 49-51.

In regard to claims 64, 94, and 115, wherein the depth of the doped heavy body is .5 microns. See col. 4, lines 3-5.

In regard to claims 65, 95, and 116, wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5 to 1.5 microns. Figure 3 depicts this range since region 14 is 2.5 microns and heavily doped region 18 extends at least half way of the region 34. See col.3, lines 15-19 and fig. 3.

In regard to claim 70, wherein the doped well has a depth less than the first depth of the gate-forming trenches. See fig.3.

In regard to claim 84, wherein between a pair of adjacent trenches a plurality of doped source regions 20 are positioned on opposite sides of each trench, and wherein the heavy body is bounded by the pair of adjacent trenches and the doped source regions. See fig. 3, for example.

In regard to claim 86, Hshieh further discloses a layer 24 of dielectric material lining inside walls of each of said plurality of gate-forming trenches; and

a layer of conductive material 22, gate, substantially filling the gate-forming trenches. See col. 3, lines 21-26.

In regard to claim 87, wherein the layer of conductive material comprises polysilicon. See col. 3, lines 24-25.

In regard to claims 47, 69, and 98, the device as mentioned above further inherently discloses that location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor. For instance, the depth of the abrupt junction significantly changes in order to control the current that passes through the channel of the device. It should be noted that the electrical field

which inherently occurs there in is controlled relatively by the magnitude of the current. For example, when an external voltage is applied at the gate of the device, it excites electrons to move in one direction creating a current in a reverse direction therein. The electric field, however, is created. Therefore, to control the electric filed it is inherently to control the current. The current is controlled by the concentration and the thickness of the channel of the transistor. See also, col. 4, lines 15-30.

In regard to claim 118, fig. 1 shows the deep dope region 16 extending into the substrate to a depth below the trench.

4. Claims 53, 59, and 74-83, 85, 88, 90-91, 96, 104, 110, and 119-120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh and Burr as applied to claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, and 92-95, 97-103, 105-109, 111-113, and 118 above, and further in view of Williams et al. (US 6,204,533, previously cited, hereinafter, Williams.)

In regard to claims 53, 88, and 104, Hshieh and Burr disclose all of the claimed limitations as mentioned above and further disclose that the trench is lined up with a dielectric material 24 and filled with conductive material 22, fig. 3. Hshieh and Burr, however, do not expressly disclose that the conductive material is recessed relatively to the surface of the substrate.

Williams, in fig. 3, for example, discloses an analogous device that includes substrate 300, doped region 302 with a first conductivity type (n-type), heavily doped region 317, and deep trenches 304. These trenches are filled with conductive material and coated with an insulating layer 306B. The trenches are recessed relatively to the

surface of the substrate in order to allow the insulating layer to cover entirely the conductive layer. This layer, therefore, securely isolated from the above conductive layer 312 and active regions in the vicinity, therefore, preventing shortage that might happen among these regions, for example, the gate, the source, and wells, etc. Shorting the gate to the source would disable the device. See also, col. 4, lines 40-46.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to imbed a recess on the conductive area as taught by Williams in Hshieh's (and Burr's) device to further secure the conductive layer as discussed above in order to prevent electrically short circuit that would disable the MOSFET.

In regard to claims 59, 74, 76, 78, and 110, Hshieh discloses all of the claimed limitations. Hshieh further discusses termination region surrounding the device, or gate-forming trenches. Since Hshieh does not explicitly show this termination region in the drawings, the Office assumes that Hshieh does not expressly disclose the depth of this termination region such substantially the same depth (this could be a little deeper since the term substantially relatively does not describe the exact number) as the transistor trench.

Williams, in fig. 3, for example, discloses an analogous device that includes substrate 300, doped region 302 with a first conductivity type (n-type), heavily doped region 317, and deep trenches 304, a deep well 316 that functions as a termination region surrounding the device that has a depth extends to substantially the same depth as the transistor trench. This depth trench operates to reduce the strength of the electric

field across the gate oxide at the corners of the trenches and limit the formation of hot carriers in the vicinity of the trench. See also, col. 4, line 66- col. 5, line 5.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize the teaching of the deep termination region as taught by Williams to incorporate this feature in Hshieh's device in order to operates to reduce the strength of the electric field across the gate oxide at the corners of the trenches and limit the formation of hot carriers in the vicinity of the trench.

In regard to claims 75 and 119, P region 613 adjacent to n-region 302 forms a p/n junction inherently. See Williams' fig. 3.

In regard to claim 77, Williams further discloses a layer of dielectric material 314 formed over the deep doped region; and

a layer of conductive material 312 formed on top of the layer of dielectric material.

The dielectric material layer is used to ensure short circuit between the source and the gate. And the conductive layer is used to deliver current and tie the deep p+ diffusion region to N+ source region. This feature is commonly used in this vertical trench gate device.

Therefore, it would have been obvious to one of ordinary skill in the at the time of the invention was made to recognize the commonly used features as taught by Williams in order to properly make connections between layers and protect the device from being electrically short.

In regard to claim 79, see above discussions regarding to claims 57-59.

In regard to claims 80-81, and 85, Williams further discloses all regions extend along the trench, See fig. 5.

In regard to claim 82, Hshieh further discloses comprising a source contact region defined at the surface of the semiconductor substrate and configured to contact the doped source region by layer 30. See also, fig. 3 and col. 5, lines 44-48.

In regard to claim 83, wherein the source contact regions are alternately formed. See fig. 3.

In regard to claim 90, see the above discussion regarding to claim 60, where Hshieh teaches the thickness of the second doped region.

In regard to claim 91, see the above discussion regarding to claim 61, where Hshieh teaches the thickness of the second doped region.

In regard to claim 96, see the above discussion regarding to claim 66, where Hshieh teaches the thickness of the distance between the bottom of the doped heavy body to the junction.

5. Claims 66 and 114-117 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hshieh and Burr as applied to claims 46-52, 54-58, 60-65, 67-73, 84, 86-87, 89, and 92-95, 97-103, 105-109, 111-113, and 118 above.

In regard to claims 66 and 114-117, Hshieh and Burr disclose all of the claimed limitations as mentioned above except explicitly mention the thickness, or distance of the heavily doped body to the doped well junction that is less than 0.5 microns. Hshieh, however, discloses the well region which contains the heavily doped region is 2.5 microns. See the above discussion regarding to claim 65.

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the thickness of this region because applicant has not disclosed that this thickness provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform equally well with either shape because they perform the same function of promoting electrical contacts between regions, in this case, regions 14 and layer 30.

Therefore, it would have been obvious to one of ordinary skill in the art to modify Hshieh to obtain the invention as specified in the above claim.

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934.

In regard to claim 120, see above discussion regarding to claim 55.

Response to Arguments

6. Applicant's arguments with respect to claims 46-120 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Nathan W. Ha/
Primary Examiner, Art Unit 2814